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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/678,609	10/04/2000	HIROKAZU HONDA	PF-2683/NEC/US/mh	7187

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EXAMINER
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ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 11/12/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/678,609	HONDA, HIROKAZU	
	Examiner	Art Unit	
	David E Graybill	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 September 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-59 and 80-85* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-59 and 80-85* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 6,7 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

In the Information Disclosure Statement filed on 8-5-2, reference AA was inadvertently lined-through. Reference AA has been considered and correctly cited on the attached Notice of References Cited.

In the rejections infra, reference labels are generally recited only for the first recitation of identical claim language.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 5-10, 12-15 and 80-85 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hurwitz (6280640), or in the alternative, over the combination of Hurwitz (6280640) and Perkins (5239448).

At column 4, lines 23-29, column 5, line 24 to column 6, line 31, column 7, lines 56-58, column 8, lines 32-37, column 9, lines 8-10, 30 and 48-52, and column 10, lines 7-9 and 30-33, Hurwitz teaches the following:

1. A semiconductor device comprising an interconnection board 18 having first and second surfaces; and a high rigidity (inherently high enough to maintain "high flatness") plate 12 securely fixed to and directly in contact with at least a majority of said second surface of said interconnection board, said high rigidity plate being equal in rigidity to said interconnection board for suppressing said interconnection board from being bent upon receipt of any stress applied during at least a process for manufacturing said interconnection board.

2. The semiconductor device as in 1, wherein said interconnection board comprises a multilayer interconnection board having a multilevel interconnection structure 14, 16.

3. The semiconductor device as in 1, wherein said high rigidity plate is made of a metal.

5. The semiconductor device as in 1, wherein said high rigidity plate is made of a ceramic.

6. The semiconductor device as in 1, wherein a base material of said interconnection board is an organic insulative material.

7. The semiconductor device as in 6, wherein said organic material is a polymer resin material.

8. A semiconductor device comprising an interconnection board having first and second surfaces; at least one semiconductor chip mounted on said first surface of said interconnection

board; and a high rigidity plate securely fixed to and directly in contact with at least a majority of said second surface of said interconnection board, said high rigidity plate being equal in rigidity to said interconnection board for suppressing said interconnection board from being bent upon receipt of any stress applied during at least a process for manufacturing said interconnection board, and for mounting said at least one semiconductor chip on said first surface.

9. The semiconductor device as in 8, wherein said interconnection board comprises a multilayer interconnection board having a multilevel interconnection structure.

10. The semiconductor device as in 8, wherein said high rigidity plate is made of a metal.

12. The semiconductor device as in 8, wherein said high rigidity plate is made of a ceramic.

13. The semiconductor device as in 8, wherein a base material of said interconnection board is an organic material.

14. The semiconductor device as in 13, wherein said organic material is a polymer resin material.

15. The semiconductor device as in 8, wherein said at least semiconductor chip is indirectly bonded via bumps 19 to said second surface of said interconnection board.

80. A semiconductor device comprising: an interconnection board having first and second surfaces; at least one external electrode pad 20 buried in said interconnection board, said at least one external electrode pad having an exposed surface level with said second surface so that said second surface and said exposed surface form a single flat plane; and a high rigidity plate securely fixed to and directly contact with at least a majority of said single flat plane, said high rigidity plate being at least equal in rigidity to the interconnection board and suppressing said interconnection board from being bent.

81. The semiconductor device as in 80, wherein said high rigidity late is securely fixed to and directly in contact with an entirety of said single flat plane.

82. A semiconductor device comprising: an interconnection board having first and second surfaces; at least one external electrode pad buried in said interconnection board, said at least one external electrode pad having an exposed surface level with said second surface so that said second surface and said exposed surface form a single flat plane; at least a semiconductor chip mounted on said first surface of said interconnection board; a high rigidity plate securely fixed to and directly in contact with at least a majority of said single flat plane, said high rigidity plate being equal in rigidity to

said interconnection board and suppressing said interconnection board from being bent.

83. The semiconductor device as claimed in 82, wherein said high rigidity plate is securely fixed to and directly contact with an entirety of said single flat plane.

84. The semiconductor device as claimed in 1, wherein said high rigidity plate is securely fixed to and directly contact with said second surface.

85. The semiconductor device as claimed in 8, wherein said high rigidity plate is securely fixed to and directly contact with an entirety of said second surface.

To further clarify the teaching of said high rigidity plate for suppressing said interconnection board from being bent upon receipt of any stress applied during at least a process for manufacturing said interconnection board, and for mounting said at least one semiconductor chip on said first surface, it is noted that this limitation is a statement of intended use of the product which does not result in a structural difference between the claimed product and the product of Hurwitz. Further, because the product of Hurwitz has the same structure as the claimed product, it is inherently capable of being used for the intended use, and the statement of intended use does not patentably distinguish the claimed product from the product of

Hurwitz. Similarly, the manner in which a product operates is not germane to the issue of patentability of the product; Ex parte Wikdahl 10 USPQ 2d 1546, 1548 (BPAI 1989); Ex parte McCullough 7 USPQ 2d 1889, 1891 (BPAI 1988); In re Finsterwalder 168 USPQ 530 (CCPA 1971); In re Casey 152 USPQ 235, 238 (CCPA 1967). Also, "Expressions relating the apparatus to contents thereof during an intended operation are of no significance in determining patentability of the apparatus claim."; Ex parte Thibault, 164 USPQ 666, 667 (Bd. App. 1969). And, "Inclusion of material or article worked upon by a structure being claimed does not impart patentability to the claims."; In re Young, 25 USPQ 69 (CCPA 1935) (as restated in In re Otto, 136 USPQ 458, 459 (CCPA 1963)). And, claims directed to product must be distinguished from the prior art in terms of structure rather than function. In re Danley, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does [or is intended to do]." Hewlett-Packard Co. v. Bausch & Lomb Inc., 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

However, Hurwitz does not appear to explicitly teach that the high rigidity plate is higher in rigidity than the interconnection board.

Regardless, as cited, Hurwitz teaches that the high rigidity plate is at least inherently equal in rigidity to the

interconnection board (because they are coextensive and integral). Moreover, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed relative rigidity limitation because applicant has not disclosed that the limitation is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical, and it appears prima facie that the process would possess utility using another rigidity. Indeed, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See MPEP 2144.05(II): "Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. '[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.'" In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also In re Hoeschele, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969), Merck & Co. Inc. v. Biocraft Laboratories Inc., 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S.

975 (1989), and In re Kulling, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990). As set forth in MPEP 2144.05(III), "Applicant can rebut a prima facie case of obviousness based on overlapping ranges by showing the criticality of the claimed range. 'The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range.' In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990). See MPEP § 716.02 - § 716.02(g) for a discussion of criticality and unexpected results."

In the alternative, Perkins teaches wherein a high rigidity plate 40 is higher in rigidity than an interconnection board ["locally complex area (MCM)"] for suppressing the interconnection board from being bent upon receipt of any stress applied during at least a process for manufacturing the interconnection board, and for mounting at least one semiconductor chip 28 on a first surface. In addition, it would have been obvious to combine the product of Perkins with the product of Hurwitz because it would reduce device stress.

Claims 4 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hurwitz or the combination of Hurwitz and Perkins as applied to claims 1-3, 5-10, 12-15 and 80-85, and further in combination with Farquhar (6329713).

Hurwitz and/or Perkins do not appear to explicitly teach the following:

4. The semiconductor device as in 1, wherein said high rigidity plate is made of an alloy.

11. The semiconductor device as in 8, wherein said high rigidity plate is made of an alloy.

Notwithstanding, at column 3, line 64 to column 4, line 1; and column 4, lines 36-67, Farquhar teaches wherein a high rigidity plate 8 is made of an alloy ["Invar"]. Moreover, it would have been obvious to combine the product of Farquhar with the product of the applied prior art because it would provide a high rigidity metal plate.

Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hurwitz or the combination of Hurwitz and Perkins as applied to claims 1-3, 5-10, 12-15 and 80-85, and further in combination with Tsukamoto (5841194).

Hurwitz and/or Perkins do not appear to explicitly teach the following:

16. The semiconductor device as in 15, wherein further comprising a sealing resin material provided on said first surface of said interconnection board for sealing said at least semiconductor chip and said bumps.

17. The semiconductor device as in 16, further comprising at least a heat spreader provided on said at least semiconductor chip.

Still, at column 4, line 59 to column 8, line 61, Tsukamoto teaches a sealing resin 205 material provided on a first surface of an interconnection board 101 for sealing a semiconductor chip and bumps 204, and a heat spreader 701 provided on the semiconductor chip. In addition, it would have been obvious to combine the product of Tsukamoto with the product of the applied prior art because it would improve manufacturing yield.

Claims 18-20, 22-37, 43, 44, 50-53 and 55-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Allen (4705205) and Hayashi (JP11238972).

At column 1, line 10 to column 2, line 20; column 2, lines 46 to column 2, line 68; column 3, lines 42-49; column 4, lines 1-21; column 8, lines 32-40; column 8, lines 62-68; column 12, line 22 to column 13, line 46; column 13, line 66 to column 14, line 38; column 15, lines 8-45; column 16, lines 27-39; column 16, line 52 to column 17, line 18; column 18, lines 15-20;

column 18, line 66 to column 19, line 16; column 20, lines 37-58; and column 21, lines 12-28, Allen teaches the following:

18. A semiconductor device comprising an interconnection board 32 having first and second surfaces; at least one external electrode pad 10 in said interconnection board, said at least one external electrode pad having an exposed surface; at least a semiconductor chip mounted on said interconnection board; and a buffer layer 20 having a first surface in contact with said second surface of said interconnection board and also said buffer layer having a second surface on which at least one external electrode 28 is provided, and said buffer layer providing at least one electrical contact 28 between said one external electrode pad and said at least one external electrode, and said buffer layer being capable of absorbing and/or relaxing a stress applied to said at least external electrode to make said interconnection board free from application of said stress.

20. The semiconductor device as in 18, wherein said at least external electrode comprises plural external electrodes.

22. The semiconductor device as in 18, wherein said external electrode comprises a pin electrode.

23. The semiconductor device as in 18, wherein said external electrode comprises a coil-spring electrode 62.

24. The semiconductor device as in 18, wherein said external electrode comprises a generally column shaped electrode.

25. The semiconductor device as in 24, wherein said generally column shaped electrode comprises a straight column shaped electrode which is uniform in horizontal cross sectional area from a bottom to a top thereof.

26. The semiconductor device as in 24, wherein said generally column shaped electrode comprises a center-pinched column shaped electrode which decreases in horizontal cross sectional area toward an intermediate level thereof.

27. The semiconductor device as in 18, wherein said buffer layer comprises

plural generally column shaped electrically conductive layers, each of which has a first end fixed to an external electrode pad 10 of said interconnection board and a second end directly fixed said external electrode.

28. The semiconductor device as in 27, wherein said plural generally column shaped electrically conductive layers are made of a metal.

29. The semiconductor device as in 18, wherein said buffer layer comprises plural generally column shaped electrically conductive layers, each of which has a first end fixed to an external electrode pad of said interconnection board and a second end

directly fixed said external electrode; and an stress absorption layer 22 filling gaps between said plural generally column shaped electrically conductive layers, and said stress absorption layer being lower in rigidity than said plural generally column shaped electrically conductive layers, and said stress absorption layer surrounding said plural generally column shaped electrically conductive layers so that said stress absorption layer is in tightly contact with said plural generally column shaped electrically conductive layers.

30. The semiconductor device as in 29, wherein said plural generally column shaped electrically conductive layers are made of a metal.

31. The semiconductor device as in 29, wherein said stress absorption layer is made of an organic insulative material.

32. The semiconductor device as in 18, wherein said buffer layer comprises

plural generally column shaped electrically conductive layers, each of which has a first end fixed to an external electrode pad of said interconnection board and a second end directly fixed said external electrode; a supporting plate 22 having plural holes, into which said plural generally column shaped electrically conductive layers with said external electrodes are inserted, and said supporting plate extending in parallel to

said second surface of said interconnection board to form an inter-space between said supporting plate and said second surface of said interconnection board ; and a supporting sealing resin material 22 filling said inter-space and surrounding both said plural generally column shaped electrically conductive layers and parts of said external electrodes so that said supporting sealing resin material is in tightly contact with said plural generally column shaped electrically conductive layers and said parts of said external electrodes for supporting said external electrodes.

33. The semiconductor device as in 32, wherein said supporting sealing resin material is lower in rigidity than said plural generally column shaped electrically conductive layers so that said supporting sealing resin material is capable of absorbing and/or relaxing a stress applied to said external electrodes.

34. The semiconductor device as in 32, wherein said plural generally column shaped electrically conductive layers are made of a metal.

35. The semiconductor device as in 32, wherein said supporting sealing resin material is made of an organic insulative material.

36. The semiconductor device as in 18, further comprising a supporting layer 34 on said second surface of said buffer layer for supporting said external electrode.

37. The semiconductor device as claimed in 36, wherein said supporting layer further comprises: a supporting plate 22 having plural holes into which holes said external electrodes are inserted, and said supporting plate extending in parallel to said second surface of said buffer layer to form an inter-space between said supporting plate and said second surface of said buffer layer; and a supporting sealing resin material 22 filling said inter-space and surrounding parts of said external electrodes so that said supporting sealing resin material is in tight contact with said parts of said external electrodes for supporting said external electrodes.

43. A semiconductor device comprising an interconnection board having first and second surfaces; at least a semiconductor chip mounted on said interconnection board; at least one external electrode fixed to said at least one external electrode pad; and a supporting layer 22 on said second surface of said interconnection board for supporting said external electrodes.

44. The semiconductor device as in 43, further comprising: a buffer layer 20 having a first surface in contact with said second surface of said interconnection board, and wherein said

supporting layer further comprises a supporting plate 22 having plural holes into which holes said external electrodes are inserted, and said supporting plate extending in parallel to said second surface of said buffer layer to form an inter-space between said supporting plate and said second surface of said buffer layer; and a supporting sealing resin material 22 filling said inter-space and surrounding parts of said external electrodes so that said supporting sealing resin material is in tight contact with said parts of said external electrodes for supporting said external electrodes.

50. The semiconductor device as in 43, wherein said external electrodes connected through plural generally column shaped electrically conductive layers to external electrode pads on said second surface of said interconnection board, and said supporting layer further comprises a supporting plate 22 having plural holes, into which said plural generally column shaped electrically conductive layers with said external electrodes are inserted, and said supporting plate extending in parallel to said second surface of said interconnection board to form an inter-space between said supporting plate and said second surface of said interconnection board; and a supporting sealing resin material 22 filling said inter-space and surrounding both said plural generally column shaped electrically conductive

layers and parts of said external electrodes so that said supporting sealing resin material is in tightly contact with said plural generally column shaped electrically conductive layers and said parts of said external electrodes for supporting said external electrodes.

51. The semiconductor device as in 50, wherein said supporting sealing resin material is lower in rigidity than said plural generally column shaped electrically conductive layers so that said supporting sealing resin material is capable of absorbing and/or relaxing a stress applied to said external electrodes.

52. The semiconductor device as in 50, wherein said plural generally column shaped electrically conductive layers are made of a metal.

53. The semiconductor device as in 50, wherein said supporting sealing resin material is made of an organic insulative material.

55. The semiconductor device as in 43, wherein said external electrode comprises a pin electrode.

56. The semiconductor device as in 43, wherein said external electrode comprises a coil-spring electrode.

57. The semiconductor device as in 18, wherein said external electrode comprises a generally column shaped electrode.

58. The semiconductor device as in 24, wherein said generally column shaped electrode comprises a straight column shaped electrode which is uniform in horizontal cross sectional area from a bottom to a top thereof.

59. The semiconductor device as in 24, wherein said generally column shaped electrode comprises a center-pinched column shaped electrode which decreases in horizontal cross sectional area toward an intermediate level thereof.

However, Allen does not appear to explicitly teach the external electrode pad buried in the interconnection board, and having the exposed surface level with the second surface so that the second surface and the exposed surface form a single flat plane, or the following:

19. The semiconductor device as in 18, wherein said interconnection board comprises a multilayer interconnection board having a multilevel interconnection structure.

Nonetheless, in the English abstracts and figures, Hayashi teaches an external electrode pad 2 buried in an interconnection board 1, and having the exposed surface level with a second surface so that the second surface and the exposed surface form a single flat plane, wherein the interconnection board comprises a multilayer interconnection board having a multilevel interconnection structure. Furthermore, it would have been

obvious to combine the product of Hayashi with the product of Allen because it would provide an interconnection board.

Claims 21, 38-42, 45-49 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Allen and Hayashi as applied to claims 18-20, 22-37, 43, 44, 50-53 and 55-59, and further in combination with Tsukamoto.

The combination of Allen and Hayashi does not appear to explicitly teach the following:

21. The semiconductor device as in 18, wherein said external electrode comprises a solder ball.

38. The semiconductor device as in 18, wherein said at least semiconductor chip is bonded via bumps to said first surface of said interconnection board.

39. The semiconductor device as in 38, wherein further comprising a sealing resin material provided on said first surface of said interconnection board for sealing said at least semiconductor chip and said bumps.

40. The semiconductor device as in 39, further comprising at least a heat spreader provided on said at least semiconductor chip.

41. The semiconductor device as in 38, wherein further comprising an under-fill resin material provided on said first

surface of said interconnection board for sealing said at least semiconductor chip and said bumps.

42. The semiconductor device as in 41, further comprising a stiffener extending on a peripheral region of said buffer layer; and at least a heat spreader provided on said at least semiconductor chip and on said stiffener.

45. The semiconductor device as in 43, wherein said at least semiconductor chip is bonded via bumps to said first surface of said interconnection board.

46. The semiconductor device as in 45, wherein further comprising a sealing resin material provided on said first surface of said interconnection board for sealing said at least semiconductor chip and said bumps.

47. The semiconductor device as in 46, further comprising at least a heat spreader provided on said at least semiconductor chip.

48. The semiconductor device as in 45, wherein further comprising an under-fill resin material provided on said first surface of said interconnection board for sealing said at least semiconductor chip and said bumps.

49. The semiconductor device as claimed in 48, further comprising: stiffener extending on a peripheral region of said

buffer layer; and at least a heat spreader provided on said at least semiconductor chip and on said stiffener.

54. The semiconductor device as in 43, wherein said external electrode comprises a solder ball.

Nonetheless, at column 4, line 59 to column 8, line 61, Tsukamoto teaches a semiconductor device wherein an external electrode comprises a solder ball, a semiconductor chip 201 is bonded via bumps 204 to a first surface of an interconnection board 101, a sealing resin 205 material provided on the first surface of the interconnection board for sealing the semiconductor chip and the bumps, an under-fill resin material 205 provided on the first surface of the interconnection board for sealing the at least semiconductor chip and the bumps, a stiffener 106 extending on a peripheral region of the interconnection board; and at least a heat spreader 701 provided on the semiconductor chip and on the stiffener. Moreover, it would have been obvious to combine the product of Tsukamoto with the product of the applied prior art because it would provide a chip carrier having improved manufacturing yield.

Applicant's remarks filed 9-5-2 have been fully considered and are adequately addressed in the rejection supra.

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions similar to the instant invention.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to Group 2800 Customer Service whose telephone number is 703-306-3329.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (703) 308-2947. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is 703/308-7722.

David E. Graybill
Primary Examiner
Art Unit 2827

D.G.
7-Nov-02